

## MIPS R12000 to Hit 300 MHz

### *Evolutionary Design From SGI Boosts Performance by 50%*

by Linley Gwennap

With its foundries ready to deliver 0.25-micron chips, Silicon Graphics (SGI) has used its experience with the initial 0.35-micron R10000 processor to enhance that product's internal design, eliminating performance bottlenecks and increasing efficiency. As a result, the revised 0.25-micron design, called the R12000, should deliver about 50% better performance than its 0.35-micron predecessor and up to three times its performance on certain applications. The new CPU, due to appear in systems in 1H98, will give SGI's product line its first big performance boost in two years.

The improvements in the R12000 include a larger window for reordering instructions, improved branch prediction, better support for large (4M) caches, and better handling of L2 cache misses. To avoid a critical timing path, the instruction-fetch pipeline is extended by one cycle. Many of these changes will have little effect on SPECint95, the standard measure of workstation performance, but will improve performance on the larger scientific and database workloads used by many of SGI's customers.

These incremental improvements will give high-end MIPS customers significantly better performance, particularly on these larger applications. The R12000 is likely to lag the SPEC ratings of leading processors from HP and Digital in 1H98, however. SGI expects faster versions of the R12000 to appear as early as 1H99, but the next big jump in performance, particularly for bandwidth-limited applications, won't come until the processor known as the H2 appears in the year 2000.

The R12000 recently taped out, and SGI is awaiting first silicon from its foundries, NEC and Toshiba. Both MIPS chip vendors plan to sell the R12000 when it is ready for volume production, but neither is quoting list prices on high-end MIPS chips due to the limited number of customers. Other than SGI, only Tandem (now part of Compaq) and Siemens-Nixdorf are buying significant quantities of R10000 chips, and these vendors have already begun converting their product lines from MIPS to Intel processors.

### Improved Branch Prediction Needed

SGI's first goal was to improve the clock speed of the R10000. Although that chip was announced at 200 MHz, yields at that clock speed have been small despite two years of effort; most of the chips yield at about 180 MHz. The new 0.25-micron version of the R10000 (see MPR 10/6/97, p. 5) operates at 250 MHz; for the R12000 to reach its 300-MHz target, some redesign was required. Missing the goal by even 10% is not acceptable; because SGI's system designs are largely synchronous, this shortfall would reduce the speed of the cache, system bus, and other buses in the system.

SGI engineers discovered a critical speed path in the R10000's instruction-fetch cycle. The R12000 adds an extra stage to the front of the pipeline, providing more time for this critical operation. With this change, and other minor circuit-design tweaks, SGI hopes the R12000 will deliver plenty of yield at 300 MHz and possibly higher.

As Figure 1 shows, the downside of this change is an increase in the branch-misprediction penalty. To compensate, SGI quadrupled the size of the branch-history table (BHT) from 512 to 2,048 entries, reducing the number of mispredictions. To access the BHT, the R12000 uses a Gshare algorithm, in which the program counter is XORed with an

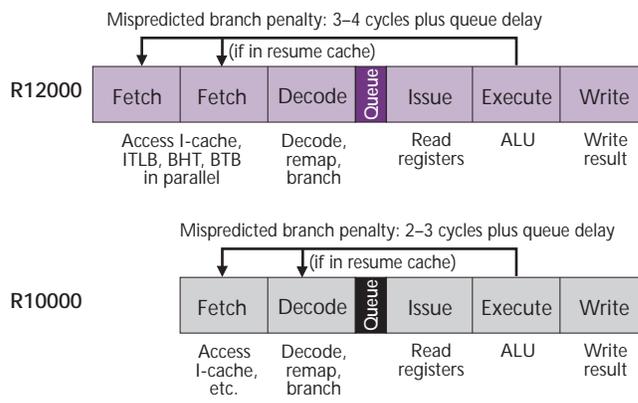


Figure 1. The R12000 extends the instruction-fetch pipeline by one stage, adding a cycle to the mispredicted branch penalty.

8-bit global branch-history register to generate the index. According to McFarling (see [www.research.digital.com/wrl/techreports/abstracts/TN-36.html](http://www.research.digital.com/wrl/techreports/abstracts/TN-36.html)), this algorithm is nearly as accurate as most two-level algorithms (see MPR 3/27/95, p. 17) but is less complex to implement in hardware.

The R10000 (see MPR 10/24/94, p. 18) is unusual among high-performance processors in not predicting the target of branches. Instead, the processor relies on the out-of-order core to hide the one-cycle latency required to calculate branch targets. Applications with lots of branches and relatively little parallelism encountered performance problems with this design, however, so the R12000 sports a small branch-target buffer. This BTB has 32 entries and is two-way set associative to reduce thrashing. Branches that miss the BTB are handled as in the R10000.

### Instruction Reordering Avoids Bottlenecks

The R10000 is an aggressive out-of-order design that has a 32-entry “active list” that keeps track of all instructions that have been dispatched but not retired; three 16-entry instruction queues, one each for integer, floating-point, and memory instructions; and integer and floating-point register files, each with 64 renamable registers. The queues are misnamed, for instructions can be issued from anywhere in the queue rather than in a first-in, first-out manner.

Because the active list must keep track of instructions

in all phases of execution, not just those in the queues, it can be a bottleneck in applications that have many dependencies. Floating-point applications in particular can never take full advantage of the 48 total queue entries, since the R10000’s active list has only 32 entries, but integer applications can also reach the limit of the active list if the integer and memory queues are nearly full and there are other instructions that have not yet been retired.

As Figure 2 shows, the R12000 expands the active list to 48 entries, breaking this bottleneck. This change increases the physical size of the active-list circuitry and also extends the maximum time needed to recover from an exception to 12 cycles, since the chip must unwind the active list four entries at a time in this situation.

The new design includes other minor changes in the instruction-issue logic. In situations where the memory-instruction queue is full, the R12000 can dispatch the address calculation (but not the memory access) of a load or store into the integer queue rather than stalling the entire instruction. Having the address precalculated accelerates the memory access by one cycle once it finally reaches the execution stage. This change, combined with the larger active list, will particularly help data-intensive FP applications that can now make better use of the integer queue.

To simplify its design, the R10000 did not take age into account when issuing instructions from the queues. This

simplification did not affect the vast majority of programs, but experience with R10000 systems helped SGI identify a few key applications for which an older instruction could get temporarily stuck in the queue, reducing performance. The R12000 is careful to give priority to older instructions, preventing this anomalous behavior.

### Memory Accesses Improved

Many of SGI’s customers use applications with large data sets, requiring a high percentage of loads and stores. For this reason, the R12000 includes several changes to improve performance on this type of application.

For example, in the R10000, an unresolved store (that is, a store for which the physical address has not been calculated) blocks the execution of all subsequent loads and stores to avoid the possibility of two memory accesses to the same physical address being executed out of order. This restriction is lifted in the R12000, which checks the physical addresses after they are calculated; if a match is found, the affected memory operations are reexecuted in the correct

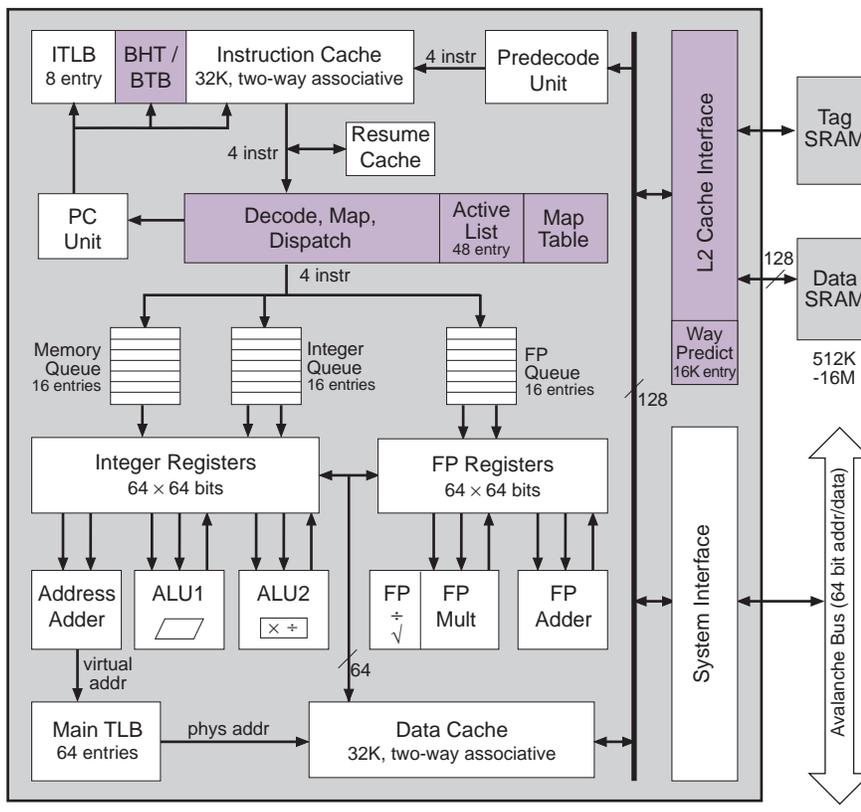


Figure 2. The R12000 microarchitecture includes a few critical changes, highlighted in purple, aimed at improving performance over that of the original R10000 design.

### Price & Availability

The R12000 will be manufactured and sold by NEC and Toshiba, with volume availability slated for 1H98. No pricing has been announced. For more information, contact SGI's MIPS Group at [www.mips.com](http://www.mips.com).

order. This change increases opportunities for parallelism among unrelated loads and stores.

The R10000 includes an unusual two-way associative level-two (L2) cache. Because the processor can access only one way (set) of this cache at a time, it predicts the desired way using a way-prediction table. In the R10000, this table has 8K entries, one for each of the lines in a 2M cache (assuming 32-word lines). For larger caches, however, each entry in the way-prediction table maps to two or more cache lines, reducing the accuracy of the prediction algorithm. Way mispredictions cause an extra cache access, reducing performance.

The R12000 doubles the size of the way-prediction table, allowing it to handle up to 4M caches without undesirable aliasing. Many SGI systems are already shipping with 4M of L2 cache today, increasing their hit rate over 2M caches, so the new chip will be better suited for these systems.

The new cache controller can service CPU accesses to the L2 cache while refilling a line in the L2 cache; in the R10000, a refill operation blocked the CPU from accessing the cache. The R12000 designers managed to trim a cycle off the latencies of a few L2 cache operations. The new chip also requires fewer penalty cycles when several L2 cache misses are pending. These and other changes will streamline the operation of the L2 cache, particularly when an application's data set overflows the cache.

One change that SGI didn't make was to expand the on-chip caches, which remain 32K each for instructions and data. SGI plans to scale the speed of the external L2 cache at the same rate as the CPU speed, reducing the need for larger L1 caches.

### 0.25-Micron Process Reduces Power, Size

MIPS vendors NEC and Toshiba will fabricate the R12000 in a 0.25-micron four-layer-metal process. Figure 3 shows the recently taped-out die, which measures 204 mm<sup>2</sup>; the final size may change slightly. Since the 0.25-micron R10000 measures 197 mm<sup>2</sup> (see MPR 10/6/97, p. 5), the new R12000 features appear to have added only 4% to the die area. Similarly, the number of transistors has increased by about 5%, from 6.8 million to 7.15 million. Most of the increase is in logic transistors, which went from 2.4 million to 2.7 million; the number of cache transistors rose slightly due to the larger way-prediction table.

The process shrink, combined with a reduction in supply voltage from 3.3 V to 2.5 V, eases power dissipation even at the higher clock speed. SGI estimates the R12000 will dissipate about 20 W (maximum) at 300 MHz, a third less

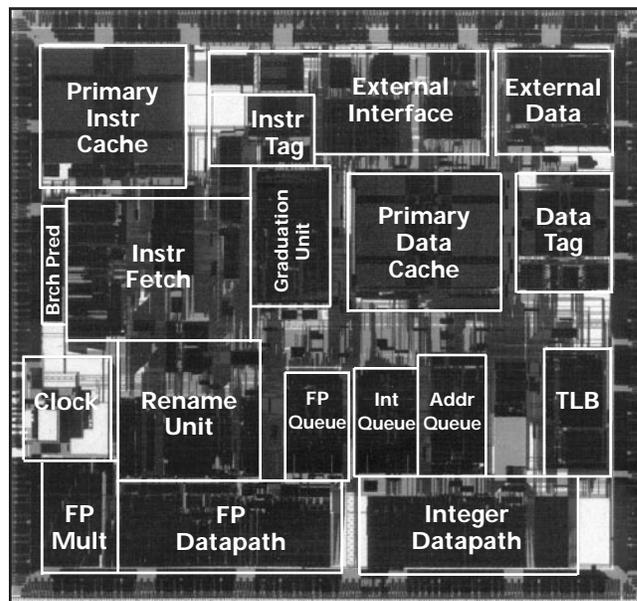


Figure 3. In a 0.25-micron four-layer-metal CMOS process, the R12000, shown in this die plot, measures 13.8 mm × 14.8 mm.

power than the 200-MHz R10000.

Although the new chip's block diagram is quite similar to that of the R10000, its physical layout has been completely changed to optimize for speed and size in the new process. The new chip, however, uses the same 527-pin ceramic PGA package as its predecessor. Other than the change in supply voltage, the chips are pin-compatible.

### Plans for the Future

The R12000 supports a variety of clock ratios for the L2 cache and the system bus. Given the limitations of system designs and the availability of high-speed SRAMs, we expect most 300-MHz R12000 systems will use a 200-MHz L2 cache and a 100-MHz system bus. In this configuration, we expect the chip will deliver about 17 SPECint95 (base) and 27 SPECfp95 (base); SGI would not provide its own performance estimates for the part.

These estimates assume the chip's performance will increase by about 50%, the same as the clock-speed jump. Although SPEC performance doesn't always scale with clock speed, the microarchitectural improvements should be enough to offset the normal declines. Applications with large data sets typically see a smaller increase when the CPU clock speed rises, but since most of the design changes target these applications, their performance may also improve by about 50%. A few applications that have severe bottlenecks on the current part may see performance gains of two or three times on the R12000.

After letting the speed of its high-end part languish for nearly two years, SGI hopes to see more rapid progress in the future. As early as 1H99, the semiconductor vendors could deliver a 0.18-micron version of the R12000 using a simple optical shrink. This part could reach clock speeds of 400 MHz or more.

In 2H99, SGI plans to deploy another version of the R12000 that is redesigned to use all six metal layers available in the 0.18-micron process. This design should reach 450 MHz or more. Although the company does not plan to modify the CPU core in this version, it may revamp the processor's bus interface to improve its bandwidth. Doubling the size of the on-chip caches might also be appropriate at this point. The company will finally move to a new core, known as the H2, in 2000 (see MPR 8/4/97, p. 4).

### R12000 Can't Match Competition

If the R12000 were shipping today, it would outstrip its competition on the SPECfp95 metric and possibly on SPECint95 as well. By the time the MIPS chip reaches the market, however, it is likely to face stronger competition, including HP's PA-8500 and Digital's 21264. Both of these processors aim to deliver in excess of 25 SPECint95 and 50 SPECfp95, leaving the R12000 in the dust.

Furthermore, the R12000 fails to address a critical weakness of the R10000: main-memory bandwidth. Due to overhead from its multiplexed design, the best sustainable bandwidth of the R12000's system bus is 674 Mbytes/s at 100 MHz. By mid-1998, the 21264 will be setting the pace with

system bandwidth of up to 2.0 Gbytes/s, and even Pentium II will be able to sustain 800 Mbytes/s using a 100-MHz bus. For applications that frequently access main memory, this bandwidth is critical to performance. SGI plans to uncork this bottleneck in 1999 or 2000.

The company's oft-delayed and ultimately canceled Beast project (see MPR 8/4/97, p. 4) left SGI in need of a stopgap solution. More than just a simple processor shrink but less than a new core, the R12000 strives admirably but won't be able to match the performance of more advanced processors from Digital and HP, even with the planned rapid migration to 0.18-micron technology. In fact, we wouldn't be surprised to see the 0.35-micron 21264 outperform the 0.18-micron R12000, albeit with a much larger die.

Fortunately for SGI, the company has made its mark with outstanding graphics accelerators and multiprocessor systems. These capabilities should continue to be strengths and, in at least some markets, mask any performance shortcomings of the R12000. And the company's new Intel-based strategy (see MPR 10/6/97, p. 23) provides a backup plan should the MIPS line fail to deliver. Thus, though the R12000 provides a needed performance boost, Silicon Graphics' key to success remains its namesake system technology. □