Examen Parcial de "Disseny de Microprocessadors"

2 de novembre de 2005

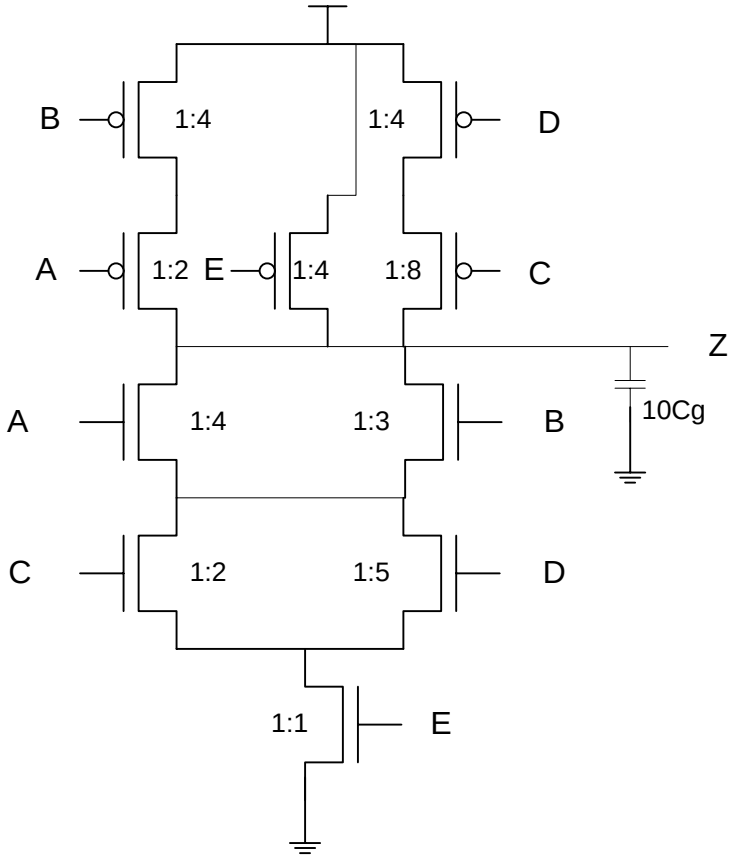
- Duration: 2h.
- You can bring your notes.
- You may use a calculator

Problem 1 (2 points)

Design the following function in CMOS and nMOS logic. Size the transistors to the appropriate dimensions for the nMOS case considering that 1Rsp = 2 Rs.

$$S = \overline{(AB + C)\cdot(D + E)}$$

Problem 2 (3 points)



Given the circuit above,

a) What function does it calculate? (Boolean expression)
b) Compute the delay for the following cases (consider $1R_{sp} = 2R_s$):
   i. A=0, B=0, C=1, D=1, E=0
   ii. A=1, B=0, C=1, D=1, E=1
   iii. A=0, B=1, C=1, D=0, E=1
c) Compute the dynamic power consumption (in watts) if the inputs change 80% of the time, the frequency is 3GHz, 1Cg = 0.9 fF i Vdd = 1,2 V.

Problem 3 (3 points)

Given a circuit that has to load an external capacity of 130fF,

a. What solution will you propose to reduce the time it takes to load (Tpf)? (1Cg=0.9fF).
b. What solution will you propose to reduce the value of the following function? (just check for f=3)

$$F(T, A, P) = 0'5 \times T + 0'2 \times A + 0'3 \times P$$

- T is the total time –delay- (in τ) of the solution.
- A is the global area of the solution (in λ) – consider N=6λ and the area of a transistor is the one of its source, drain (that we consider the same size) plus the gate. ($A_{transistor} = 2 \times W \times N + L \times W$)
- P is the total power consumption measured as the internal capacity of the circuit (in Cg) –meaning without the input and output capacitances..

Problem 4 (2 points)

Sketch the layout in pseudo n-MOS for a standard cell that implements the following function:

$$S = \overline{(AB + CD)E}$$