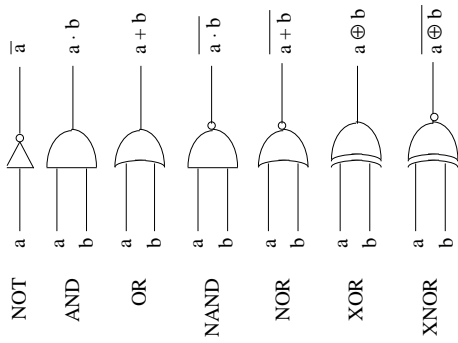


# INTRODUCCIÓ ALS COMPUTADORS

Xuletari de circuits digitals

## PORTES LÒGIQUES

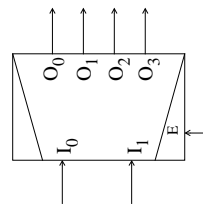


|   |     |
|---|-----|
| a | NOT |
| 0 | 1   |
| 1 | 0   |

| a | b | AND | OR | NAND | NOR | XOR | XNOR |
|---|---|-----|----|------|-----|-----|------|
| 0 | 0 | 0   | 0  | 1    | 1   | 0   | 1    |
| 0 | 1 | 0   | 1  | 1    | 0   | 1   | 0    |
| 1 | 0 | 0   | 1  | 1    | 0   | 1   | 0    |
| 1 | 1 | 1   | 1  | 0    | 0   | 0   | 1    |

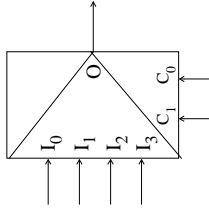
## BLOCS COMBINATORIS

DECODIFICADOR (2 a 4)



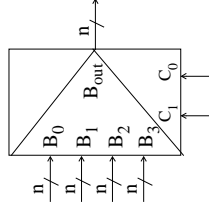
| E | I <sub>1</sub> | I <sub>0</sub> | O <sub>3</sub> | O <sub>2</sub> | O <sub>1</sub> | O <sub>0</sub> |
|---|----------------|----------------|----------------|----------------|----------------|----------------|
| 0 | x              | x              | 0              | 0              | 0              | 0              |
| 1 | 0              | 0              | 0              | 0              | 0              | 1              |
| 1 | 0              | 1              | 0              | 0              | 1              | 0              |
| 1 | 1              | 0              | 0              | 1              | 0              | 0              |
| 1 | 1              | 1              | 1              | 0              | 0              | 0              |

MULTIPLEXOR (4 a 1)



| C <sub>1</sub> | C <sub>0</sub> | O              |
|----------------|----------------|----------------|
| 0              | 0              | I <sub>0</sub> |
| 0              | 1              | I <sub>1</sub> |
| 1              | 0              | I <sub>2</sub> |
| 1              | 1              | I <sub>3</sub> |

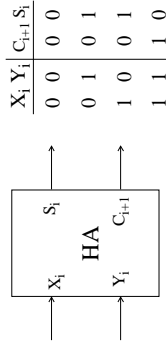
MULTIPLEXOR DE BUSES (4 a 1)



| C <sub>1</sub> | C <sub>0</sub> | B <sub>out</sub> |
|----------------|----------------|------------------|
| 0              | 0              | B <sub>0</sub>   |
| 0              | 1              | B <sub>1</sub>   |
| 1              | 0              | B <sub>2</sub>   |
| 1              | 1              | B <sub>3</sub>   |

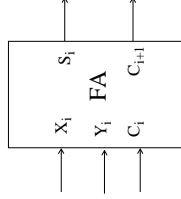
SUMADORS

Semisumador



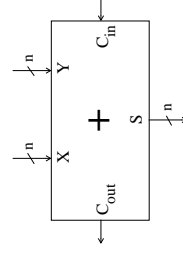
| X <sub>1</sub> | X <sub>2</sub> | S <sub>1</sub> | C <sub>1+1</sub> |
|----------------|----------------|----------------|------------------|
| 0              | 0              | 0              | 0                |
| 0              | 1              | 1              | 0                |
| 1              | 0              | 1              | 0                |
| 1              | 1              | 0              | 1                |

Sumador Complet



| C <sub>i</sub> | X <sub>1</sub> | X <sub>2</sub> | S <sub>1</sub> | C <sub>1+1</sub> |
|----------------|----------------|----------------|----------------|------------------|
| 0              | 0              | 0              | 0              | 0                |
| 0              | 0              | 1              | 0              | 1                |
| 0              | 1              | 0              | 0              | 1                |
| 0              | 1              | 1              | 1              | 0                |
| 1              | 0              | 0              | 0              | 1                |
| 1              | 0              | 1              | 1              | 0                |
| 1              | 1              | 0              | 1              | 0                |
| 1              | 1              | 1              | 1              | 1                |

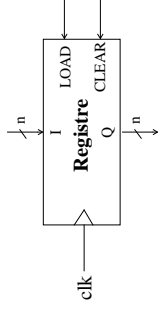
Sumador d'n bits



$$C_{out} S \leftarrow X + Y + C_{in}$$

# REGISTRE

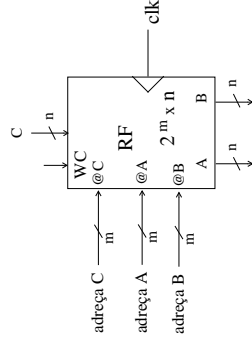
De càrrega paral·lela



Funcionament

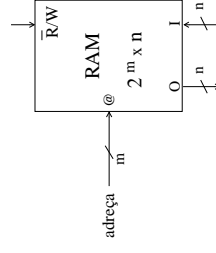
|           |               |                            |                |
|-----------|---------------|----------------------------|----------------|
| Asincron: |               | Sincron:<br>(si CLEAR = 0) |                |
| CLEAR     | Q             | LOAD                       | Q <sup>+</sup> |
| 0         | Func. sincron | 0                          | Q              |
| 1         | 0             | 1                          | I              |

# BANC DE REGISTRES



$RF[C]^+ := C$  if  $WC = 1$   
 $A := RF[A]$   
 $B := RF[B]$

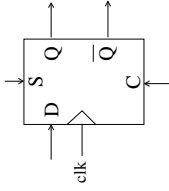
# MEMÒRIA RAM



|             |                                |
|-------------|--------------------------------|
| $\bar{R}/W$ | Funció                         |
| 0           | Lectura: $O = M[@]$            |
| 1           | Esctura: $M[@] = I$<br>$O = x$ |

# BLOCS SEQÜENCIALS

## BIESTABLE D SINCRONITZAT PER FLANC (FLIP-FLOP D)



Funcionament asincron

|   |   |               |
|---|---|---------------|
| S | C | Q             |
| 0 | 0 | Func. sincron |
| 0 | 1 | 0             |
| 1 | 0 | 1             |
| 1 | 1 | Prohibit      |

Funcionament sincron (si  $S=0$  i  $C=0$ )  $\Rightarrow$   $Q^+ := D$

|   |   |   |                |   |
|---|---|---|----------------|---|
| Funció de transició:<br>(si $S=0$ i $C=0$ ) |   | D | Q <sup>+</sup> | D |
| 0   | 0 | 0 | 0              | 0 |
| 1   | 1 | 1 | 1              | 1 |

|  |   |   |                |   |
|--|---|---|----------------|---|
| Funció d'excitació:<br>(si $S=0$ i $C=0$ ) |   | Q | Q <sup>+</sup> | D |
| 0  | 0 | 0 | 0              | 0 |
| 0  | 1 | 0 | 1              | 1 |
| 1  | 0 | 1 | 0              | 0 |
| 1  | 1 | 1 | 1              | 1 |

|                                       |                            |                            |
|---------------------------------------|----------------------------|----------------------------|
| I = Input                             | HA = Half Adder            | S = Set                    |
| O = Output                            | FA = Full Adder            | C = Clear                  |
| B = Bus                               | S = Sum                    | RF = Register File         |
| E = Enable                            | C = Carry                  | WC = Write C               |
| C <sub>1</sub> = Control <sub>1</sub> | clk = Clock                | RAM = Random Access Memory |
|                                       | $\bar{R}/W$ = Read / Write |                            |